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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,226	12/10/2003	William M. Hiatt	10829744US	8010

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EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,226	HIATT ET AL.	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,28-37 and 39-53* is/are pending in the application.

4a) Of the above claim(s) *12-14 and 37* is/are withdrawn from consideration.

5)☒ Claim(s) *28-36,39-47 and 49-52* is/are allowed.

6)☒ Claim(s) *1-11 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/19/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Embodiment 2 corresponding to Figures 5A-5B in the reply filed on 06/21/2006 is acknowledged.

The restriction requirement mailed 04/18/2008 is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 9-10, and 48 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka).

Regarding claim 1: Hayasaka discloses a method of forming a conductive interconnect in a microelectronic device (examples in Figures 7A-7I, 8-9, 13A-13C,14A-14D,17A-17B, 33, and 34A-34C), the method comprising:

providing a microfeature workpiece (Fig 33 element 152) having a plurality of dies (Fig 33 element 151_2, 151_3);

forming an open passage (Fig 14A, element 13) extending through the microfeature workpiece from a first side of the microfeature workpiece to an opposite second side of the microfeature workpiece (col 16 lines 42-45);

after forming the passage, forming a conductive plug (Fig 7D element 15; Fig 13B element 29; Fig 17A element 15; Figs 33,34A-34C element 104) in the passage adjacent to the first side of the microelectronic workpiece; and

depositing conductive material (Fig 13C element 30; Fig 17B element 8; Figs 33, 34A-34C element 156) in the passage to at least generally fill the passage from the conductive plug to the second side of the microelectronic workpiece.

Regarding claim 9: Hayasaka discloses the method of claim 1, further comprising applying a passivation layer (Fig 7C,14,17B element 14) to at least a portion of the passage before forming the conductive plug in the passage and filling the passage from the conductive plug to the second side of the microelectronic workpiece (Fig 17B).

Regarding claim 10: Hayasaka discloses the method of claim 1, further comprising forming a bond-pad (Fig 14D element 17) on the microelectronic workpiece in contact with the conductive plug.

Regarding claim 48: Hayasaka discloses the method of claim 1, further comprising applying a passivation layer (Fig 7C,14,17B element 14) to at least a portion of the passage (Fig 14A, element 13) before forming the conductive plug (Fig 7D element 15; Fig 13B element 29; Fig 17A element 15; Figs 33,34A-34C element 104) in the passage, and wherein depositing conductive material (Fig 13C element 30; Fig 17B

element 8; Figs 33, 34A-34C element 156) in the passage to at least generally fill the passage includes depositing the conductive material in contact with the conductive plug and the passivation layer (see Fig 13C, 17B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 7,045,015 to Renn et al. (Renn).

Regarding claim 2, Hayasaka discloses the method of claim 1, as above, and forming a conductive plug by depositing an electrically conductive material in the passage. Hayasaka lacks disclosing depositing an electrically conductive material by using a maskless mesoscale materials deposition process. Renn discloses using a maskless mesoscale materials deposition process to deposit an electrically conductive material (col 8 lines 24-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the electrically conductive material deposited by a maskless mesoscale materials deposition process as in Renn because the process can deposit fine features on low-temperature or high-temperature substrates (col 2 lines 22-25).

Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pub. No. 2004/0087441 to Hirakata et al. (Hirakata).

Regarding claim 3, Hayasaka discloses the method of claims 1 as above. Hayasaka lacks disclosing forming a conductive plug includes applying an electronic ink in the passage using an electronic printing process. Hirakata teaches forming a conductive plug includes applying an electronic ink (conductive paste; paragraph 102) in the passage using an electronic printing process (ink jetting; paragraph 102). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive e plug by applying an electronic ink using an electronic printing process as in Hirkata because with electronic printing processes the plug only needs to be formed in the desired area therefore wasted material is reduced.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pub. No. 2004/0087441 to Bock et al. (Bock).

Regarding claim 4, Hayasaka discloses the method of claims 1 as above. Hayasaka fails to disclose depositing an electrically conductive material in the passage using a nano-particle deposition process. Bock teaches using a nano-particle process to deposit a conductive material (abstract lines 15-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to

have the electrically conductive material deposited by a nano-particle process as in Bock because the process can deposit fine features.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 6,828,223 to Chuang.

Regarding claim 5, Hayasaka discloses the method of claim 1 where forming a conductive plug includes depositing a metal into the passage (col 12 lines 56-57). Hayasaka fails to disclose the metal as silver. Chuang teaches using silver as a conductive plug (col 1 lines 11-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the metal be silver as in Chuang because silver has low-resistivity and is a good electrical conductor.

Claims 6-8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino).

Regarding claim 6, Hayasaka discloses the method of claim 1, further comprising forming a bond-pad (Fig 14D element 17) on the microelectronic workpiece and forming the passage (Fig 14D element 13). Hayasaka fails to disclose wherein forming the open passage includes forming the open passage through the bond-pad, and wherein forming a conductive plug in the passage includes depositing a conductive material to contact an exposed surface of the bond-pad.

Mashino teaches a method of forming a conductive interconnect in a microelectronic device (Figures 1-8, element 215) further comprising forming a bond-pad (211) on the microelectronic workpiece, wherein forming the passage (212) includes forming the passage through the bond-pad (Figure 4L), and wherein forming a conductive plug in the passage includes depositing a conductive material to contact an exposed surface of the bond-pad (col 6 lines 65-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the passage through the bond-pad as in Mashino in order to have the bond pad and plug be electrically connected through the passage.

Regarding claim 7, Hayasaka discloses the method of claim 1. Hayasaka fails to discloses where forming the open passage includes laser drilling the open passage through the die. Mashino teaches where forming the passage includes laser drilling (Figure 4L, col 9 line 37- col 10 line 4) the passage through the die. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to form the passage using laser drilling to cleanly form the passage.

Regarding claim 8, Hayasaka discloses the method of claim 1 where providing a microfeature workpiece includes providing a die having an integrated circuit (integrated circuit within element 11 shown in Figure 9) and a bond-pad (Fig 14D element 17) electrically coupled to the integrated circuit.

Hayasaka fails to disclose wherein forming the passage (212) includes laser drilling (Figure 4L, col 9 line 37- col 10 line 4) the passage through the die and the bond pad (col 6 lines 58-59).

Mashino teaches where providing a microfeature workpiece includes providing a die having an integrated circuit (202) and a bond-pad (211) electrically coupled to the integrated circuit (col 6 lines 50-52), and wherein forming the passage (212) includes laser drilling (Figure 4L, col 9 line 37- col 10 line 4) the passage through the die and the bond pad (col 6 lines 58-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to form the passage using laser drilling to cleanly form the passage.

Regarding claim 11, Hayasaka discloses the method of claim 1 where depositing conductive material in the passage to at least generally fill the passage (13). Hayasaka fails to discloses biasing the conductive plug at an electrical potential.

Mashino teaches wherein depositing conductive material in the passage to at least generally fill the passage includes biasing the conductive plug at an electrical potential (power feed layer 205a, can provide an electrical potential). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to biasing the conductive plug at an electrical potential as in Mashino in order to allow for device operation.

Allowable Subject Matter

Claims 28-36, 39-47 and 49-52 are allowed.

The following is an examiner's statement of reasons for allowance:

Re claim 28: the prior art fails to teach or render obvious the claim limitations including: a passage extending completely through the die and aligned with an

extending through the bond pad and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage.

Re claim 33: the prior art fails to teach or render obvious the claim limitations including: a passage extending completely through the bond pad and die and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage.

Re claim 39: the prior art fails to teach or render obvious the claim limitations including: a passage extending completely through the first die and the first bond pad and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage.

Re claim 44: the prior art fails to teach or render obvious the claim limitations including: a passage aligned with and extending through the the first bond pad and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 1-11 and 48 filed 01/30/2008 have been fully considered but they are not persuasive.

Regarding claim 1: Applicant notes that during the interview on 01/22/2008 that examiner agreed to the claimed amendments. Examiner notes that the interpretation of "open passage" can be considered with respect to the above rejection. The term open passage does not require extension through the entire workpiece substrate or the bond pad.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is

(571)272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A. M./
Examiner, Art Unit 2811

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811